



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|--------------------------------------|-------------|----------------------------|---------------------|------------------|
| 10/520,331 | 01/04/2005 | Eduard Ferninand Stikvoort | NL02 0622 US | 5112 |
| 65913 | 7590 | 08/01/2008 | EXAMINER | |
| NXP, B.V. | | | SINGH, HIRDEPAL | |
| NXP INTELLECTUAL PROPERTY DEPARTMENT | | | ART UNIT | PAPER NUMBER |
| M/S41-SJ | | | 2611 | |
| 1109 MCKAY DRIVE | | | | |
| SAN JOSE, CA 95131 | | | | |
| NOTIFICATION DATE | | DELIVERY MODE | | |
| 08/01/2008 | | ELECTRONIC | | |

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

| | | | |
|------------------------------|------------------------|---------------------|--|
| Office Action Summary | Application No. | Applicant(s) | |
| | 10/520,331 | STIKVOORT ET AL. | |
| | Examiner | Art Unit | |
| | HIRDEPAL SINGH | 2611 | |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 17 April 2008.
 2a) This action is FINAL. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-5 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1-5 is/are rejected.
 7) Claim(s) _____ is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ . |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____. | 6) <input type="checkbox"/> Other: _____ . |

DETAILED ACTION

1. This action is in response to the amendment filed on April 17, 2008. Claims 1-5 are pending and have been considered below.

Response to Arguments

2. Applicant's argument that "The current application is a U.S. National Stage application. The labeling of figures with text matter is prohibited under PCT Rule 11.11, except when absolutely indispensable for understanding. Further, MPEP 1893.03(f) states that "[t]he USPTO may not impose requirements beyond those imposed by the Patent Cooperation Treaty...Applicants respectfully assert that additional text labeling is not required in the drawings of the current application."

3. The Applicant seems to be misinterpreting the PCT Rule 11.11 that states:

11.11 *Words in Drawings*

- (a) The drawings shall not contain text matter, except a single word or words, when absolutely indispensable, such as "water," "steam," "open," "closed," "section on AB," and, in the case of electric circuits and block schematic or flow sheet diagrams, a few short catchwords indispensable for understanding.
- (b) Any words used shall be so placed that, if translated, they may be pasted over without interfering with any lines of the drawings.

It is clearly described (PCT rule 11.11) above, that in case of electrical circuits a few catchwords required (indispensable) for understanding shall be contained in the drawings. As in the present case, figure 1 has some boxes with absolutely no symbolical representation. One has to refer back and forth to the specification to figure

out what those boxes represent. Therefore, to make it clear and easy to understand, in case this application is published as a US Patent, the above mentioned figure needs to have descriptive labels. Therefore, the objection to the drawings is upheld.

4. Applicant's arguments with respect to claims 1-5 have been considered but are moot in view of the new ground(s) of rejection.

Drawings

5. The drawing figure 1 is objected to because there are no labels for blocks 1-7. These blocks need to have descriptive labels under 37 CFR 1.84(n) and 1.84(o). For example, "BPF" may be used for the label of block number 1.

Claim Objections

6. Claims 1-5 are objected to because of the following informalities: All the limitations in a claim should be separated by semicolons not by a comma. It is suggested that a colon (:) is inserted in line 3 of claim 1 after "the arrangement comprising". At the end of the limitations a semicolon should be inserted e.g. in claim 1 line 4 the comma after "...bandwidth of the channel" be replaced with a semicolon. Appropriate correction is required.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claims 1 and 3-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hajimiri et al. (US 2002/0173337) in view of Cheung (US 6,476,685) further in view of Chappell (US 2002/0141494).

Regarding claim 1:

Hajimiri discloses tuning arrangement for receiving a plurality of signal channels and for tuning (paragraph 0066) to a specific of said plurality of signal channels, the arrangement comprising:

a polyphase mixer (432 in figure 8; paragraph 0070) for mixing said specific signal channel to an intermediate frequency (paragraphs 0016 and 0073) which is lower than twice the bandwidth of the channel;

a polyphase IF filter (460 in figure 8) for rejecting the negative frequencies in the mixer output signal (paragraphs 0009, 0011 and 0073).

Hajimiri discloses all of the subject matter as described above except for specifically teaching; (1) an intermediate frequency which is lower than twice the bandwidth of the channel; and (2) a polyphase group delay equalizer connected to the output of the polyphase IF filter characterized in that the transfer function of the group delay equalizer has, for the frequency range of interest, one or more pole-zero pairs

alongside of only the positive imaginary axis of the complex frequency plane with the pole(s) and the zero(s) of said one or more pairs lying substantially symmetrically with respect to said positive imaginary axis, wherein the one or more pole zero pairs are shifted along the positive imaginary axis off of the real axis of the complex frequency plane.

However, regarding item (1) above, Chappell in same field of endeavor discloses a system and method for determining frequency response in cable TV systems where mixer is mixing said specific signal channel to an intermediate frequency which is lower than the bandwidth of the channel (paragraph 0045; figure 3).

Therefore, it would have been obvious to one of ordinary skill in the art the time of invention to use a tuning arrangement for selecting a specific channel by mixing the local oscillator frequency to the signal channel where the oscillator frequency is lower than twice the channel bandwidth in order to make the baseband signal frequency less than of equal to the center frequency of the preceding filter circuitry to make the response of the system desirable by getting the signal frequency lying between the cutoff frequencies of the filter circuits.

Regarding item (2) above, Cheung in same field of endeavor discloses using a group delay equalizer (abstract) and the transfer function of the equalizer has, for the frequency range of interest, only one or more pole-zero pairs alongside of the positive imaginary axis of the complex frequency plane (figure 4a) with the pole(s) and the zero(s) of said one or more pairs lying substantially symmetrically with respect to said positive imaginary axis (figure 4b).

Therefore, it would have been obvious to one of ordinary skill in the art the time of invention to implement a group delay equalizer as taught by Cheung in the channel selection or tuning system of Hajimiri in order to keep the delay at a lower and invariable amount as the transfer function with poles and zeros symmetrical to the positive imaginary axis has the advantage that this arrangement compensates for the delay introduced by the filtering components as they introduce more delay at low frequencies than at high frequencies, the delay equalizer compensate for that by having more delay to high frequencies than lower frequencies.

Regarding claim 3:

Hajimiri discloses all of the subject matter as described above except for specifically teaching that a cascade of group delay equalizers is connected to the output of the polyphase IF filter, each of said group delay equalizers having only one pole-zero pair alongside of the positive imaginary axis of the complex frequency plane.

However, Cheung in same field of endeavor discloses using a group delay equalizer (abstract) and further discloses cascade of group delay equalizers (column 3, lines 15-20) is connected to the output of the filter with group delay equalizers having only one pole-zero pair alongside of the positive imaginary axis of the complex frequency plane (figure 4a; column 3, lines 22-25).

Therefore, it would have been obvious to one of ordinary skill in the art the time of invention to implement a group delay equalizer as taught by Cheung in the channel selection or tuning system of Hajimiri in order to take advantage of different delay response of cascaded equalizers to compensate over a required frequency spectrum.

Regarding claims 4 and 5:

Hajimiri discloses all of the subject matter as described above except for specifically teaching that individual group delay equalizers within the cascade of group delay equalizers comprise different or same pole-zero patterns.

However, Cheung in same field of endeavor discloses using a group delay equalizer (abstract) and further discloses cascade of group delay equalizers (column 3, lines 15-20) where the pole-zero pattern of the group delay equalizers is as shown in figures 4a and figure 4b depending on the first or second order equalizer used.

Therefore, it would have been obvious to one of ordinary skill in the art the time of invention to implement a group delay equalizer as taught by Cheung in the channel selection or tuning system of Hajimiri by cascading first or second order equalizers and to one of ordinary skill it is obvious that when using two equalizer whether they are first order or second order group delay equalizers with similar components having similar characteristics the pole-zero pattern of cascaded equalizer is obtainable as desired i.e. same or different for the cascaded equalizers in order to take advantage of different delay response of cascaded equalizers to compensate over a required frequency spectrum.

4. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hajimiri et al. (US 2002/0173337) in view of Cheung (US 6,476,685) further in view of Chappell (US 2002/0141494) as applied to claim 1 above, and further in view of Sempel et al. (US 6,324,233).

Regarding claim 2:

Hajimiri discloses all of the subject matter as described above except for specifically teaching that group delay equalizer comprises an in phase part and a quadrature phase part, each of said parts comprising a balanced operational amplifier, first conductances and first capacitances connected in parallel between each output and the inverting input of the operational amplifier for constituting the pole in the complex frequency plane, second conductances between each input of the part and one of the inputs of the operational amplifier and second capacitances between each input of the part and the other of the inputs of the operational amplifier for constituting the zero in the complex frequency plane and further conductances connecting the inputs of the operational amplifier of each part to the inputs and to the outputs of the other of said parts for shifting the pole and the zero along the positive imaginary axis of the complex frequency plane.

However, Sempel in the same field of endeavor teaches a group delay equalizer (figures 5b and 5c) comprising balanced operational amplifier (A1- A4 in figure 5b), first conductances and first capacitances (G, G/4, 3.4 pF in figure 5b; column 6, lines 1-35) connected in parallel between each output and the inverting input of the operational amplifier for constituting the pole in the complex frequency plane, second conductances (as shown in figure 5b) between each input of the part and one of the inputs of the operational amplifier and second capacitances (2.5 pF in figure 5b) between each input of the part and the other of the inputs of the operational amplifier for constituting the zero in the complex frequency plane and further conductances connecting the inputs of

the operational amplifier of each part to the inputs and to the outputs of the other of said parts for shifting the pole and the zero along the positive imaginary axis of the complex frequency plane.

Therefore, it would have been obvious to one of ordinary skill in the art the time of invention to implement a group delay equalizer as taught by Sempel in the channel selection or tuning system of Hajimiri in order to make the system with less power consumption saving chip area and getting required characteristics.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.
 - a. Margairaz et al. (US 6,985,710) discloses a polyphase mixer circuit for image rejection in broadband signal reception systems.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to HIRDEPAL SINGH whose telephone number is (571) 270-1688. The examiner can normally be reached on Mon-Fri (Alternate Friday Off) 8:30AM-6:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Shuwang Liu can be reached on 571-272-3036. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/H. S./
Examiner, Art Unit 2611
/Shuwang Liu/
Supervisory Patent Examiner, Art Unit 2611